Sheet: pwr+interface

File: pwr+interface.sch

Sheet: misc-io

File: misc-io.sch

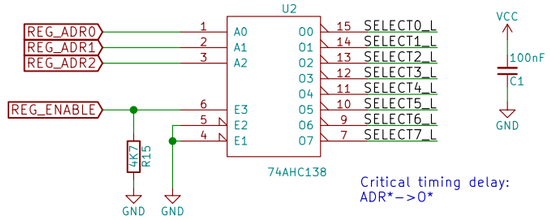
Sheet: TTL_IN_OUT

File: TTL_IN_OUT.sch

Sheet: DS8641-ARB

File: DS8641.sch

Unused driver pins on pin headers




REG_ENABLE: The 74LVTH541 input latches must not drive the shared BBB SYSBOOT pins on power-up.

Optimization BBB: Dez 2019)
RN8,9 (DATIN) : 15 Ohm
RN10 <1:6>(REGADR): 0 Ohm
RN10 <7:8>(REGWRITE): 0 Ohm
R6,R7 (REGWRITE TERM): none
RN6,RN7 (DATOUT inline): 10
RN4,RN5 /DATOUT end) -> -/-

F1 Fiducial

F2 Fiducial

Sheet: DS8641-ADR07

File: DS8641.sch

Sheet: DS8641-ADR815

File: DS8641.sch

Sheet: DS8641-ADR167+MSYN

File: DS8641.sch

Sheet: DS8641-DAT07

File: DS8641.sch

Sheet: DS8641-DAT815

File: DS8641.sch

Sheet: DS8641-SSYN+MISC

File: DS8641.sch

Sheet: /
File: unibone.sch

**Title:**

| Size: A3 | Date: | **Rev:** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 1/11 |

UNIBUS supply to BBB

UNIBUS supply to drivers

Implicite VCC is 3.3 V.
Generated on BBB.
+5VD for drivers explicit

VCC +3.3V

+5VD UB_5V C36 6.3uF C37 6.3uF C38 6.3uF C39 6.3uF GND

Supply bread board 1+2

J4 +3.3V +3.3V
J3 +5VD +5V UB
J5 GND
J34 +3.3V +3.3V
J35 +5VD +5V UB
J36 GND

BBB Header:
use 2x25 pin footprint:
cabling 50 pins!

MMC1 on P8<11:21>

J1 GND

| | | | |
|---|---|---|---|
| GPIO1_6_38 | 3 | 4 | GPIO1_7_39 |
| GPIO1_2_34 | 5 | 6 | GPIO1_3_35 |
| GPIO2_2_66 | 7 | 8 | GPIO2_3_67 |
| TIMER5 | 9 | 10 | GPIO2_4_68 |
| GPIO1_13_45 | 11 | 12 | GPIO1_12_44 |
| | 13 | 14 | |
| | 15 | 16 | GPIO1_14_46 |
| | 17 | 18 | GPIO2_1_65 |
| | 19 | 20 | PRU1_13 |
| PRU1_12 | 21 | 22 | GPIO1_5_37 |
| GPIO1_4_36 | 23 | 24 | GPIO1_1_33 |
| GPIO1_0_32 | 25 | 26 | |
| PRU1_08 | 27 | 28 | PRU1_10 |
| PRU1_09 | 29 | 30 | PRU1_11 |
| | 31 | 32 | |
| | 33 | 34 | |
| | 35 | 36 | |
| | 37 | 38 | |
| PRU1_06 | 39 | 40 | PRU1_07 |
| PRU1_04/SYSBOOT4 | 41 | 42 | PRU1_05 |
| PRU1_02/SYSBOOT2 | 43 | 44 | PRU1_03/SYSBOOT3 |
| PRU1_00/SYSBOOT0 | 45 | 46 | PRU1_01/SYSBOOT1 |

BBB-P8

Supply BBB: PDP-11 to input jack +5VA
Supply cape: 2x250mA from BBB +3.3V

J2 GND GND

| | | | |
|---|---|---|---|
| | 1 | 2 | |
| | 3 | 4 | |
| | 5 | 6 | |
| | 7 | 8 | |
| | 9 | 10 | SYSRESET_L |
| LED_BUS_ACTIVITY | 11 | 12 | PANEL_RESET_L |
| | 13 | 14 | GPIO1_18_50 |
| GPIO1_16_48 | 15 | 16 | GPIO1_19_51 |
| | 17 | 18 | |
| I2C2_SCL | 19 | 20 | I2C2_SDA |
| UART2_TXD | 21 | 22 | UART2_RXD |
| GPIO1_17_49 | 23 | 24 | UART1_TXD |
| PRU0_07 | 25 | 26 | UART1_RXD |
| PRU0_05 | 27 | 28 | PRU0_03 |
| PRU0_01 | 29 | 30 | PRU0_02 |
| PRU0_00 | 31 | 32 | |
| | 33 | 34 | |
| | 35 | 36 | |
| | 37 | 38 | |
| | 39 | 40 | |
| | 41 | 42 | |
| PRU0_06 | 43 | 44 | PRU0_04 |
| | 45 | 46 | |

BBB-P9

SYSRESET_L BTN SW3 GND

+3.3V D6 GNBUS 470 R14 LED_BUS_ACTIVITY
LED "On BUS"

+3.3V D1 PWR 470 R5 GND
LED "Power"

Global driver Output Enable

+5VD 470 R4 BUS_ENABLE_L
BUS_ENABLE 10K R2 1K R3 Q1 MMBT3904 GND

+5VA K1 HFD3 UB_5V UB_5V
1N4148WS D7
Q2 MMBT3904
R16 22K R1 1K C44 470uF GND

Override BBB boot config
Default: ...11100 = MMC1,MMC0,UART0,
...10111 = MMC0,SPI0,UART0,USB0
...10011 = NAND,NAND2C,MMC0,UART0

+3.3V
R11 22K R12 22K R13 22K GND

| |
|---|
| PRU1_00/SYSBOOT0 |
| PRU1_01/SYSBOOT1 |
| PRU1_02/SYSBOOT2 |
| PRU1_03/SYSBOOT3 |
| PRU1_04/SYSBOOT4 |

Use of PRU-EGPIOs:

RN8 15

| | | |
|---|---|---|
| PRU1_00/SYSBOOT0 | 1 | REG_DATIN_0 |
| PRU1_01/SYSBOOT1 | 3 | REG_DATIN_1 |
| PRU1_02/SYSBOOT2 | 5 | REG_DATIN_2 |
| PRU1_03/SYSBOOT3 | 7 | REG_DATIN_3 |
| PRU1_04/SYSBOOT4 | 1 | REG_DATIN_4 |
| PRU1_05 | 3 | REG_DATIN_5 |
| PRU1_06 | 5 | REG_DATIN_6 |
| PRU1_07 | 7 | REG_DATIN_7 |

RN9 15

RN10 0

| | | |
|---|---|---|
| PRU1_08 | 1 | REG_ADR0 |
| PRU1_09 | 3 | REG_ADR1 |
| PRU1_10 | 5 | REG_ADR2 |
| PRU1_11 | 7 | REG_WRITE |

PRU1_12
PRU1_13

REGADR & WRITE both best at 0 Ohm

RN6 10

| | | |
|---|---|---|
| PRU0_00 | 1 | REG_DATOUT_0 |
| PRU0_01 | 3 | REG_DATOUT_1 |
| PRU0_02 | 5 | REG_DATOUT_2 |
| PRU0_03 | 7 | REG_DATOUT_3 |
| PRU0_04 | 1 | REG_DATOUT_4 |
| PRU0_05 | 3 | REG_DATOUT_5 |
| PRU0_06 | 5 | REG_DATOUT_6 |
| PRU0_07 | 7 | REG_DATOUT_7 |

RN7 10

Use of GPIOs:

| | |
|---|---|
| GPIO1_0_32 | LED0 |
| GPIO1_1_33 | LED1 |
| GPIO1_2_34 | LED2 |
| GPIO1_3_35 | LED3 |
| GPIO1_4_36 | SW0 |
| GPIO1_5_37 | SW1 |
| GPIO1_6_38 | SW2 |
| GPIO1_7_39 | SW3 |
| GPIO1_12_44 | BUTTON |
| GPIO1_13_45 | BUS_ENABLE |
| GPIO1_14_46 | REG_ENABLE |

Reserve GPIOs:

J11

| | |
|---|---|
| GPIO1_16_48 | 1 |
| GPIO1_17_49 | 2 |
| GPIO1_18_50 | 3 |
| GPIO1_19_51 | 4 |

GPIO1_16-19

J37

| | |
|---|---|
| GPIO2_1_65 | 1 |
| GPIO2_2_66 | 2 |
| GPIO2_3_67 | 3 |
| GPIO2_4_68 | 4 |
| TIMER5 | 5 |

GPIO2_1-5

J16
CONN-DEC-QUAD-CDEF

| | | | |
|---|---|---|---|
| UB_NPG_IN_H | CA1 | CA2 | UB_5V |
| UB_NPG_OUT_H | CB1 | CB2 | UB_-15V |
| UB_PA_L | CC1 | CC2 | |
| UB_LTC | CD1 | CD2 | UB_D15_L |
| | CE1 | CE2 | UB_D14_L |
| | CF1 | CF2 | UB_D13_L |
| UB_D11_L | CH1 | CH2 | UB_D12_L |
| | CJ1 | CJ2 | UB_D10_L |
| | CK1 | CK2 | UB_D09_L |
| | CL1 | CL2 | UB_D08_L |
| | CM1 | CM2 | UB_D07_L |
| UB_DCLO_L | CN1 | CN2 | UB_D04_L |
| | CP1 | CP2 | UB_D05_L |
| | CR1 | CR2 | UB_D01_L |
| UB_PB_L | CS1 | CS2 | UB_D00_L |
| | CT1 | CT2 | UB_D03_L |
| UB_15V | CU1 | CU2 | UB_D02_L |
| UB_ACLO_L | CV1 | CV2 | UB_D06_L |

GND GND

| | | | |
|---|---|---|---|
| | DA1 | DA2 | UB_5V |
| | DB1 | DB2 | UB_-15V |
| | DC1 | DC2 | |
| | DD1 | DD2 | UB_BR7_L |
| | DE1 | DE2 | UB_BR6_L |
| | DF1 | DF2 | UB_BR5_L |
| | DH1 | DH2 | UB_BR4_L |
| | DJ1 | DJ2 | |
| | DK1 | DK2 | UB_BG7_IN_H |
| UB_INIT_L | DL1 | DL2 | UB_BG7_OUT_H |
| | DM1 | DM2 | UB_BG6_IN_H |
| | DN1 | DN2 | UB_BG6_OUT_H |
| | DP1 | DP2 | UB_BG5_IN_H |
| | DR1 | DR2 | UB_BG5_OUT_H |
| | DS1 | DS2 | UB_BG4_IN_H |
| | DT1 | DT2 | UB_BG4_OUT_H |
| | DU1 | DU2 | |
| | DV1 | DV2 | |

GND GND

| | | | |
|---|---|---|---|
| | EA1 | EA2 | UB_5V |
| | EB1 | EB2 | UB_-15V |
| UB_A12_L | EC1 | EC2 | |
| UB_A17_L | ED1 | ED2 | UB_A15_L |
| UB_MSYN_L | EE1 | EE2 | UB_A16_L |
| UB_A02_L | EF1 | EF2 | UB_C1_L |
| UB_A01_L | EH1 | EH2 | UB_A00_L |
| UB_SSYN_L | EJ1 | EJ2 | UB_C0_L |
| UB_A14_L | EK1 | EK2 | UB_A13_L |
| UB_A11_L | EL1 | EL2 | |
| | EM1 | EM2 | |
| | EN1 | EN2 | UB_A08_L |
| UB_A10_L | EP1 | EP2 | UB_A07_L |
| UB_A09_L | ER1 | ER2 | |
| | ES1 | ES2 | |
| | ET1 | ET2 | |
| UB_A06_L | EU1 | EU2 | UB_A04_L |
| UB_A05_L | EV1 | EV2 | UB_A03_L |

GND GND

| | | | |
|---|---|---|---|
| | FA1 | FA2 | UB_5V |
| | FB1 | FB2 | UB_-15V |
| | FC1 | FC2 | |
| UB_BBSY_L | FD1 | FD2 | |
| | FE1 | FE2 | |
| | FF1 | FF2 | |
| | FH1 | FH2 | |
| UB_NPR_L | FJ1 | FJ2 | |
| | FK1 | FK2 | |
| | FL1 | FL2 | |
| UB_INTR_L | FM1 | FM2 | |
| | FN1 | FN2 | |
| | FP1 | FP2 | |
| | FR1 | FR2 | |
| | FS1 | FS2 | |
| | FT1 | FT2 | UB_SACK_L |
| | FU1 | FU2 | |
| | FV1 | FV2 | |

GND GND

J60
Reichelt AKL 059-6

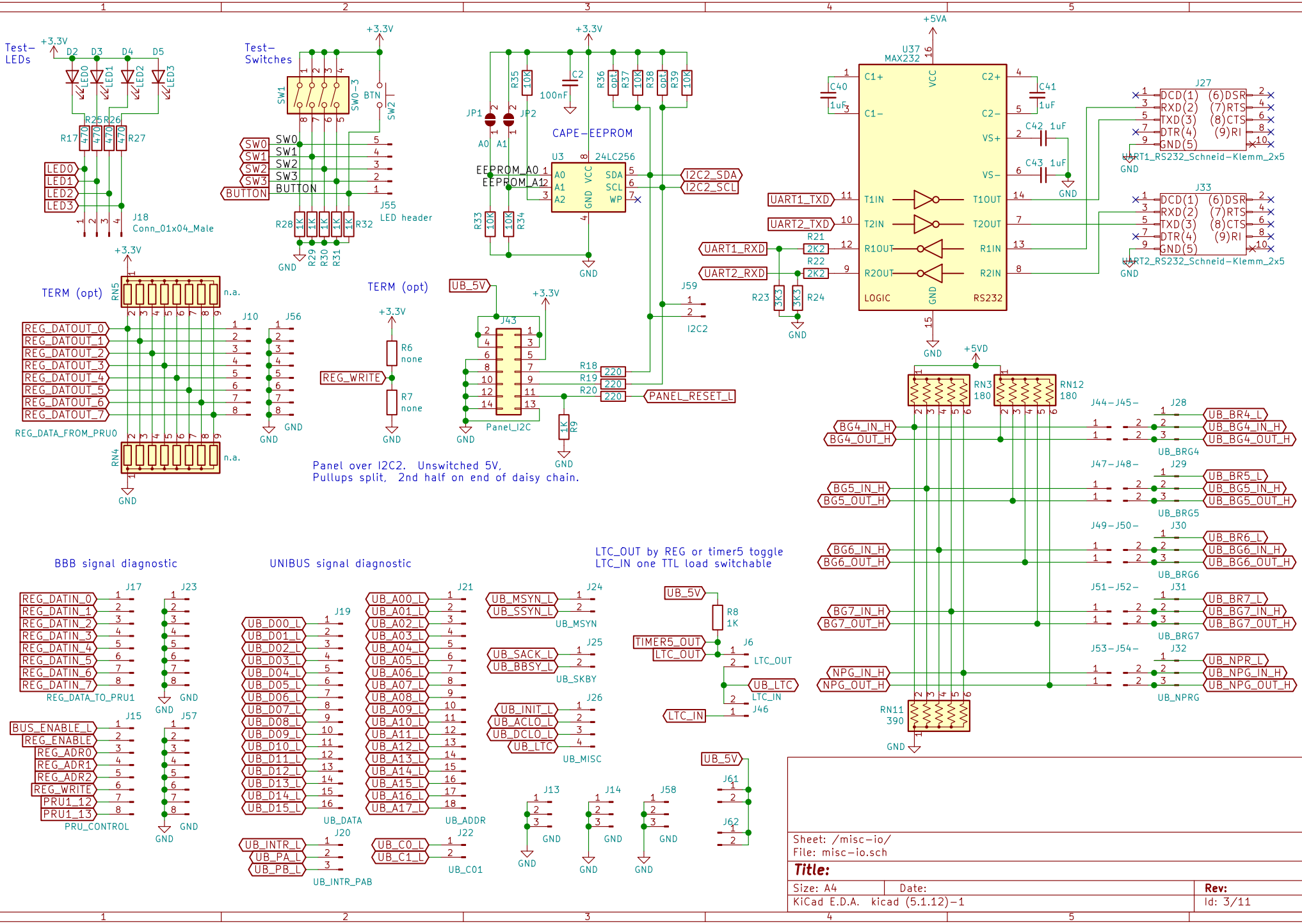
| | |
|---|---|
| UB_-15V | 6 |
| UB_15V | 5 |
| UB_5V | 4 |
| | 3 |
| | 2 |
| | 1 |

GND

Sheet: /pwr+interface/
File: pwr+interface.sch

**Title:**

| | | |
|---|---|---|
| Size: A3 | Date: | **Rev:** |
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 2/11 |


Test–
LEDs
+3.3V
D2
D3
D4
D5
LED0
LED1
LED2
LED3
R25
R26
R17
470
R27
LED0
LED1
LED2
LED3
J18
Conn_01x04_Male
Test–
Switches
+3.3V
SW1
SW0–3
BTN
SW2
SW0
SW1
SW2
SW3
BUTTON
BUTTON
J55
LED header
R28
R32
1K
R29
R30
R31
GND
+3.3V
JP1
JP2
R35
10K
C2
100nF
R36
opt
R37
10K
R38
opt
R39
10K
CAPE–EEPROM
U3
24LC256
A0
A1
A2
VCC
GND
SDA
SCL
WP
EEPROM_A0
EEPROM_A1
I2C2_SDA
I2C2_SCL
R33
10K
R34
GND
+5VA
U37
MAX232
VCC
C1+
C1–
C2+
C2–
VS+
VS–
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
LOGIC
GND
RS232
C40
1uF
C41
1uF
C42
1uF
C43
1uF
UART1_TXD
UART2_TXD
UART1_RXD
UART2_RXD
R21
2K2
R22
2K2
R23
3K3
R24
3K3
J27
DCD(1)
RXD(2)
TXD(3)
DTR(4)
GND(5)
DSR(6)
RTS(7)
CTS(8)
RI(9)
UART1_RS232_Schneid–Klemm_2x5
J33
UART2_RS232_Schneid–Klemm_2x5
TERM (opt)
RN5
n.a.
J10
J56
REG_DATOUT_0
REG_DATOUT_1
REG_DATOUT_2
REG_DATOUT_3
REG_DATOUT_4
REG_DATOUT_5
REG_DATOUT_6
REG_DATOUT_7
REG_DATA_FROM_PRU0
RN4
n.a.
GND
TERM (opt)
+3.3V
R6
none
REG_WRITE
R7
none
GND
UB_5V
+3.3V
J43
Panel_I2C
R18
R19
R20
220
PANEL_RESET_L
R9
1K
GND
J59
I2C2
Panel over I2C2. Unswitched 5V,
Pullups split, 2nd half on end of daisy chain.
+5VD
RN3
180
RN12
180
BG4_IN_H
BG4_OUT_H
J44–J45–
J28
UB_BR4_L
UB_BG4_IN_H
UB_BG4_OUT_H
UB_BRG4
BG5_IN_H
BG5_OUT_H
J47–J48–
J29
UB_BR5_L
UB_BG5_IN_H
UB_BG5_OUT_H
UB_BRG5
BG6_IN_H
BG6_OUT_H
J49–J50–
J30
UB_BR6_L
UB_BG6_IN_H
UB_BG6_OUT_H
UB_BRG6
BG7_IN_H
BG7_OUT_H
J51–J52–
J31
UB_BR7_L
UB_BG7_IN_H
UB_BG7_OUT_H
UB_BRG7
NPG_IN_H
NPG_OUT_H
J53–J54–
J32
UB_NPR_L
UB_NPG_IN_H
UB_NPG_OUT_H
UB_NPRG
RN11
390
GND
BBB signal diagnostic
J17
J23
REG_DATIN_0
REG_DATIN_1
REG_DATIN_2
REG_DATIN_3
REG_DATIN_4
REG_DATIN_5
REG_DATIN_6
REG_DATIN_7
REG_DATA_TO_PRU1
GND
J15
J57
BUS_ENABLE_L
REG_ENABLE
REG_ADR0
REG_ADR1
REG_ADR2
REG_WRITE
PRU1_12
PRU1_13
PRU_CONTROL
GND
UNIBUS signal diagnostic
J19
UB_D00_L
UB_D01_L
UB_D02_L
UB_D03_L
UB_D04_L
UB_D05_L
UB_D06_L
UB_D07_L
UB_D08_L
UB_D09_L
UB_D10_L
UB_D11_L
UB_D12_L
UB_D13_L
UB_D14_L
UB_D15_L
UB_DATA
J21
UB_A00_L
UB_A01_L
UB_A02_L
UB_A03_L
UB_A04_L
UB_A05_L
UB_A06_L
UB_A07_L
UB_A08_L
UB_A09_L
UB_A10_L
UB_A11_L
UB_A12_L
UB_A13_L
UB_A14_L
UB_A15_L
UB_A16_L
UB_A17_L
UB_ADDR
J20
UB_INTR_L
UB_PA_L
UB_PB_L
UB_INTR_PAB
J22
UB_C0_L
UB_C1_L
UB_C01
J24
UB_MSYN_L
UB_SSYN_L
UB_MSYN
J25
UB_SACK_L
UB_BBSY_L
UB_SKBY
J26
UB_INIT_L
UB_ACLO_L
UB_DCLO_L
UB_LTC
UB_MISC
LTC_OUT by REG or timer5 toggle
LTC_IN one TTL load switchable
UB_5V
R8
1K
TIMER5_OUT
LTC_OUT
J6
LTC_OUT
UB_LTC
LTC_IN
J46
LTC_IN
J13
J14
J58
GND
UB_5V
J61
J62
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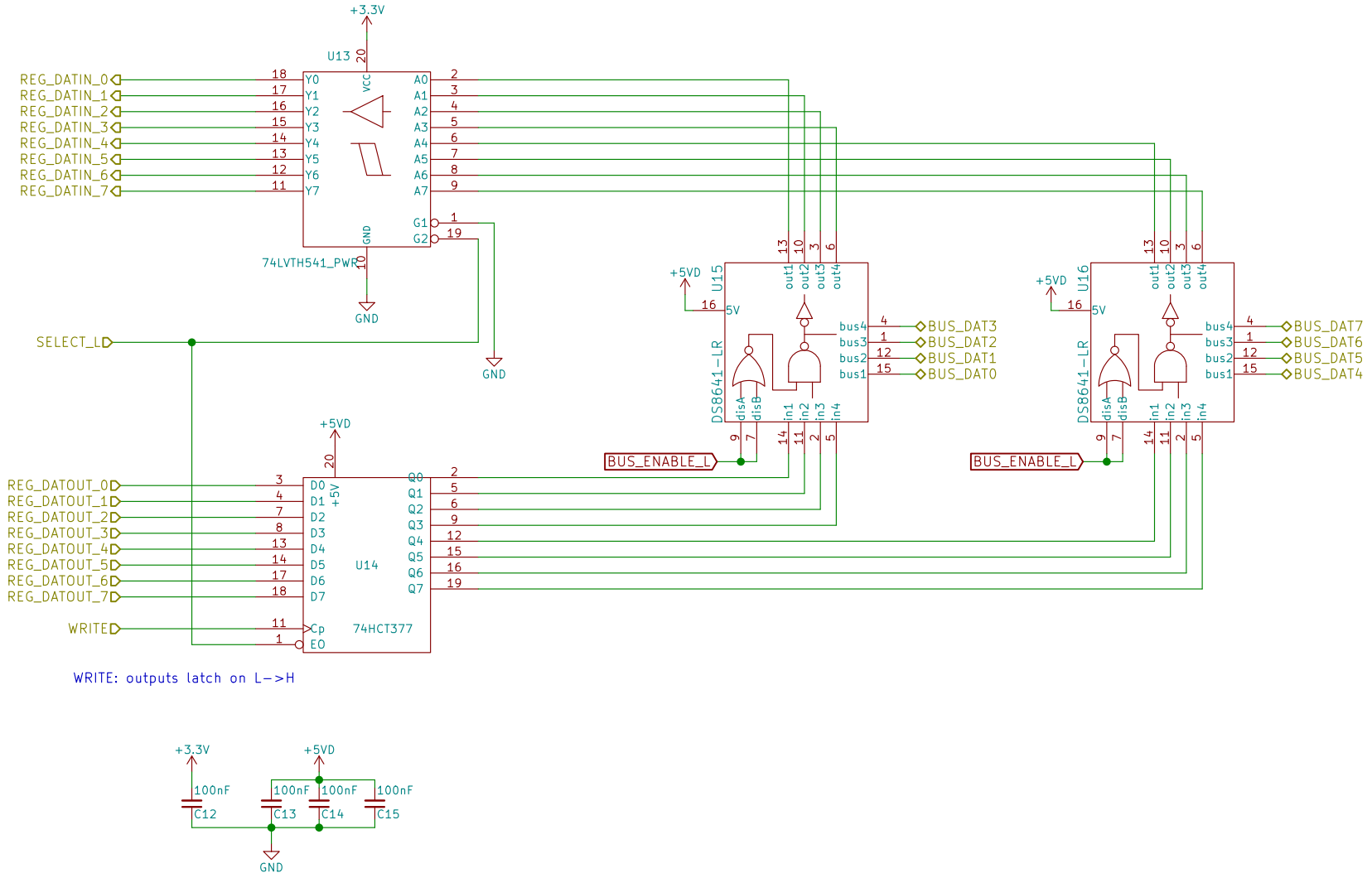
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.12)–1
Id: 3/11

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| File: DS8641.sch | | |
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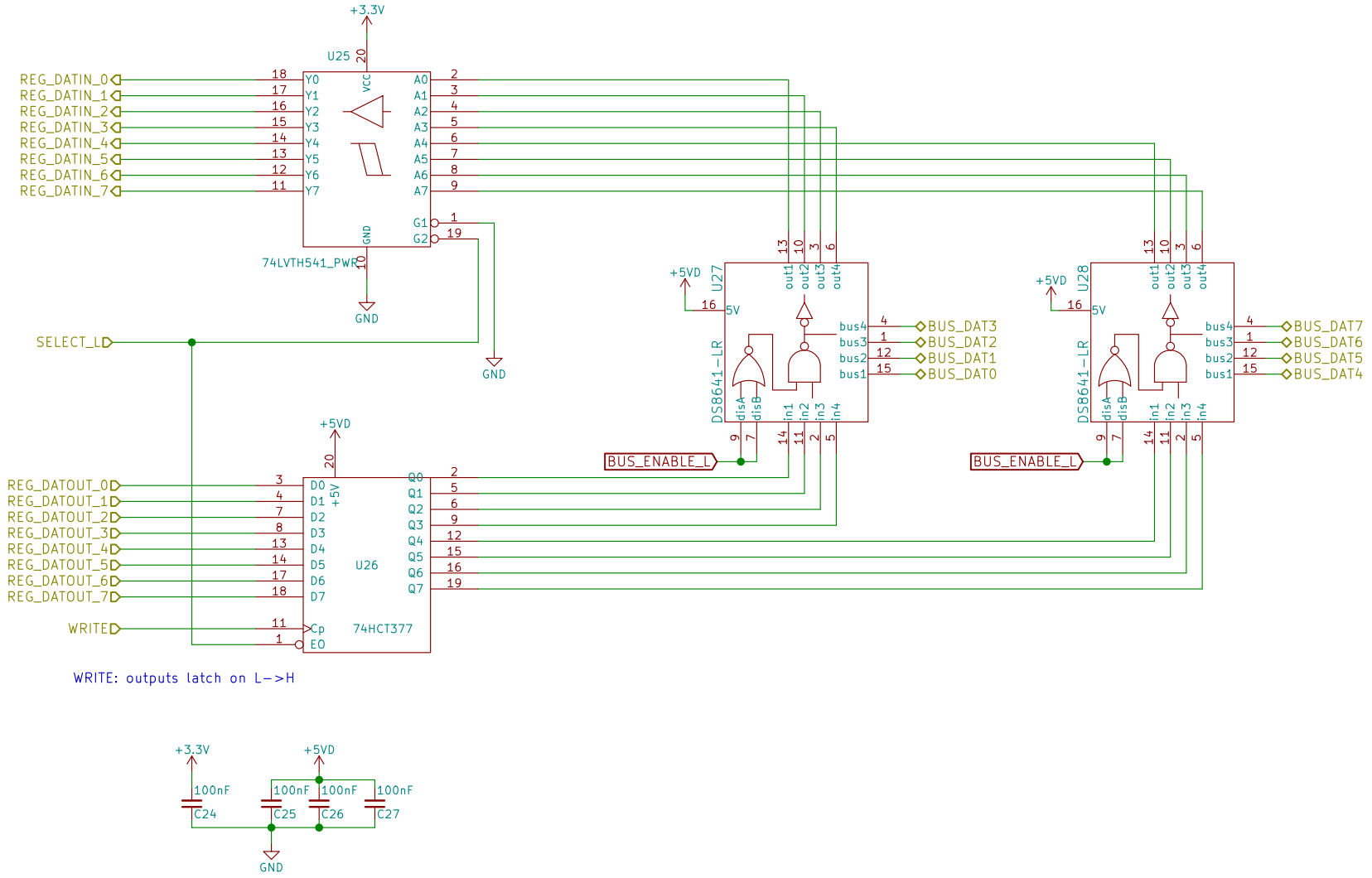
| Size: A4 | Date: | **Rev:** |
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 4/11 |

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|---|---|---|
| Sheet: /DS8641-ADR167+MSYN/ | | |
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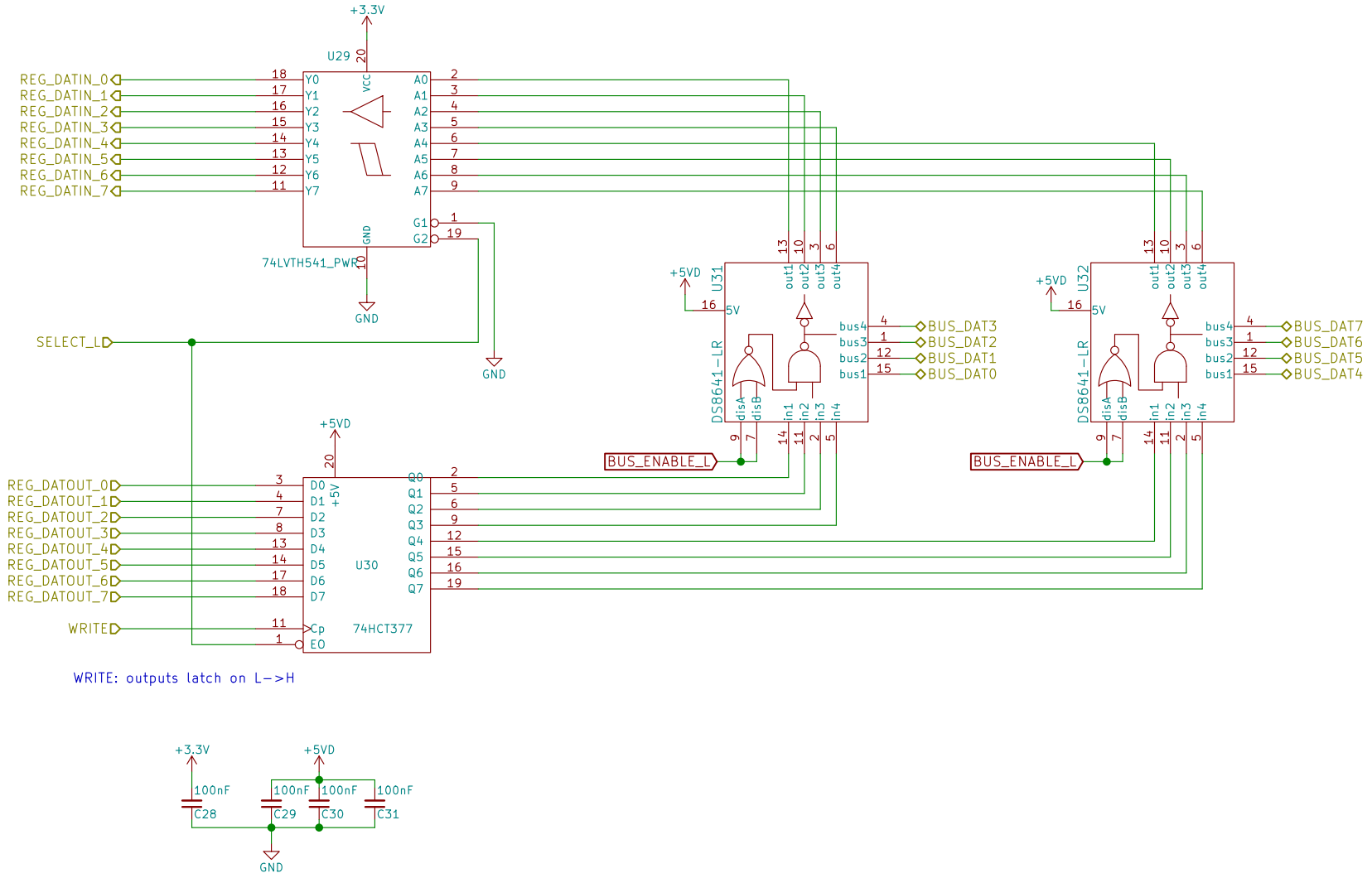


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File: DS8641.sch

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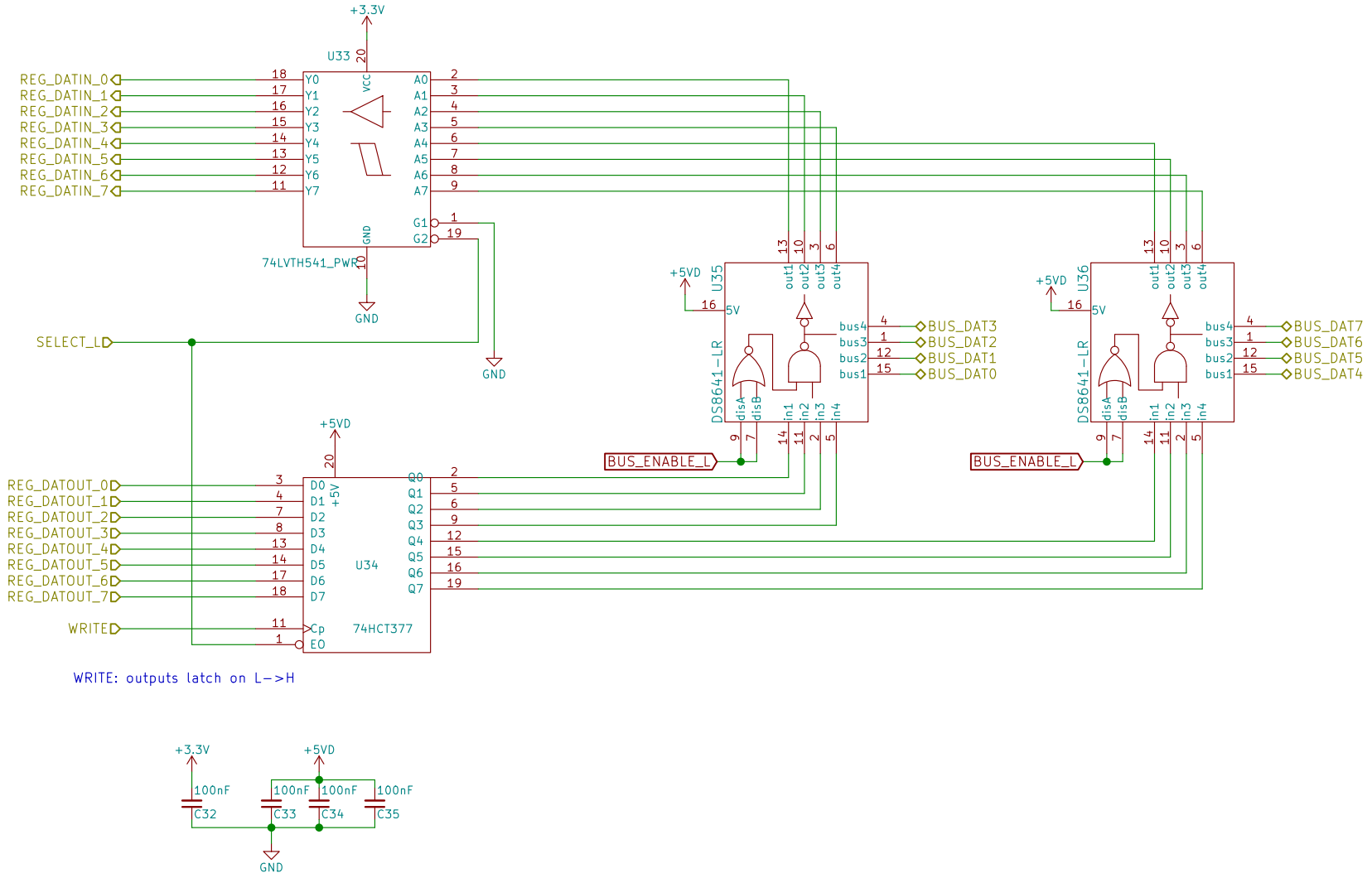


Sheet: /DS8641-SSYN+MISC/
File: DS8641.sch

**Title:**

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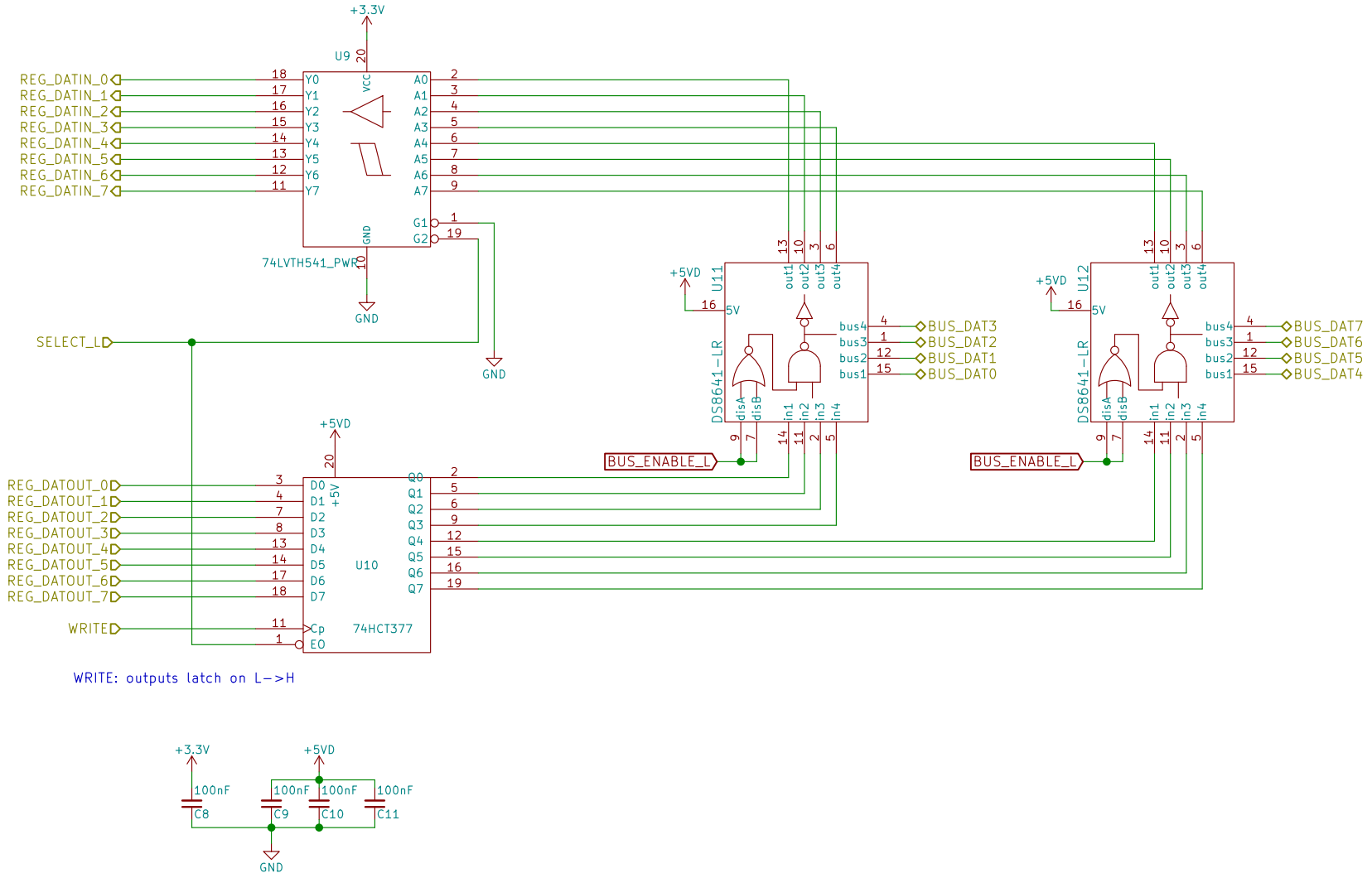
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 7/11 |




| | | |
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| Sheet: /DS8641-ADR07/ | | |
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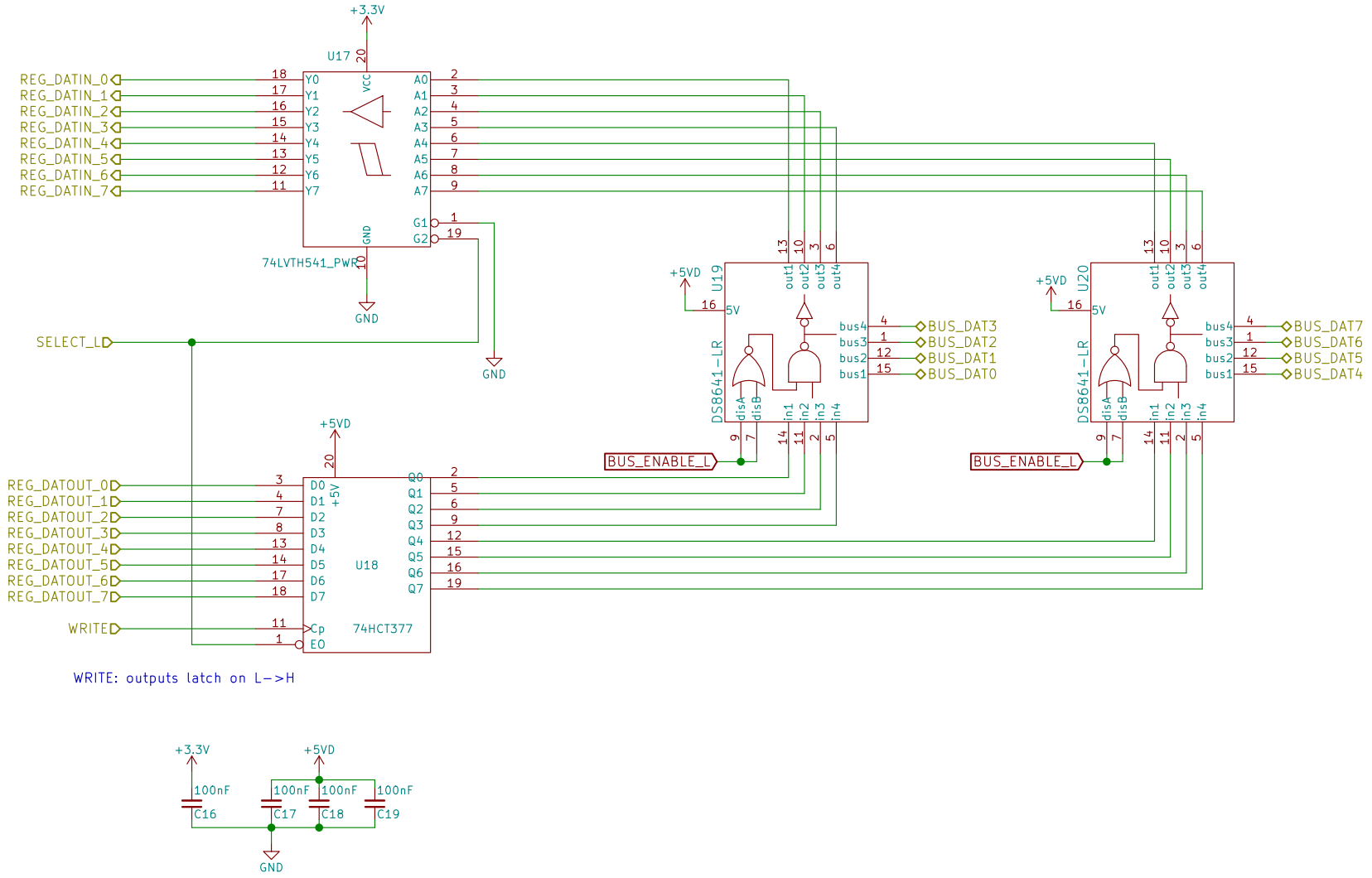
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 8/11 |




| | | |
|---|---|---|
| Sheet: /DS8641-DAT07/ | | |
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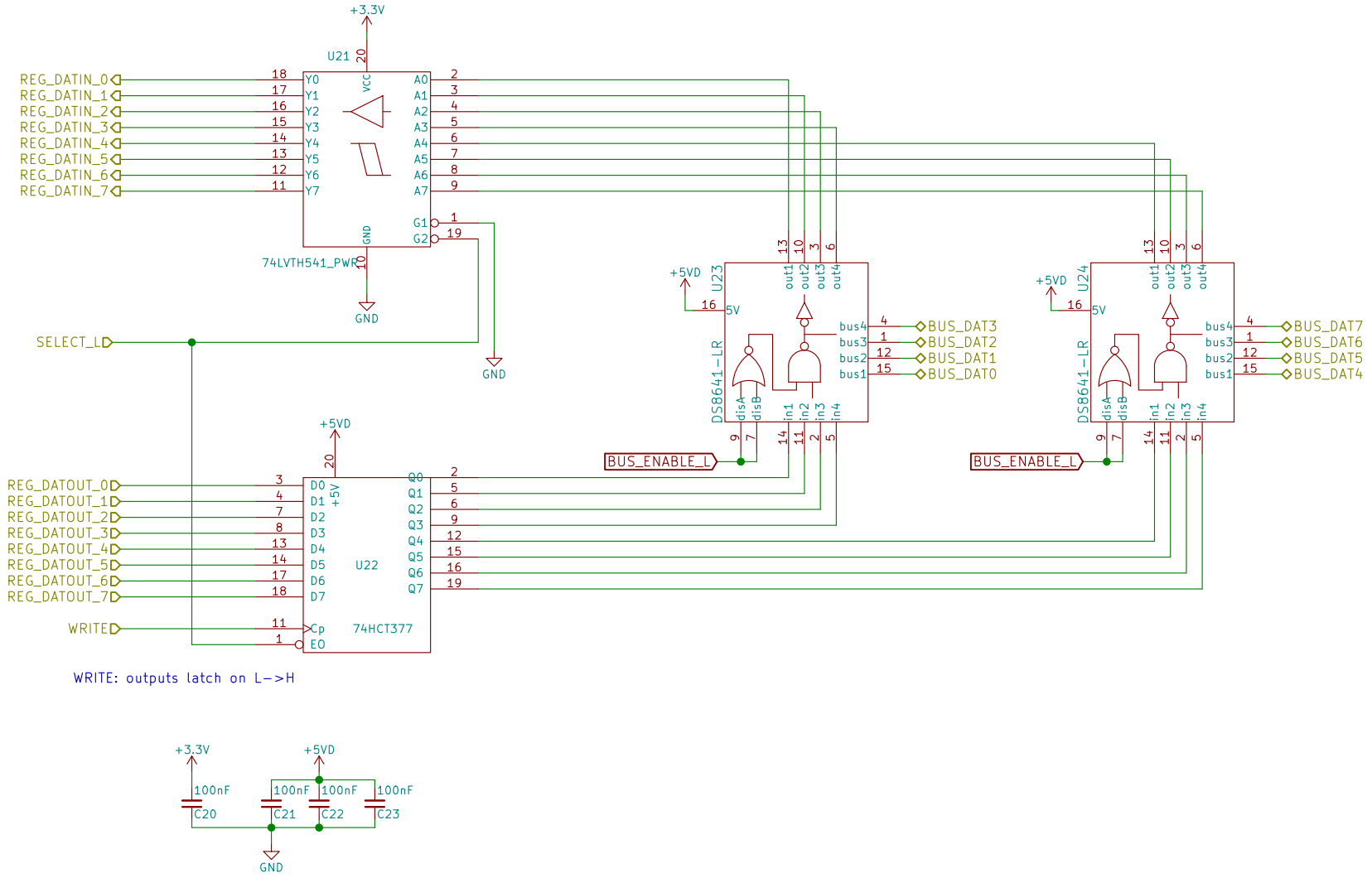


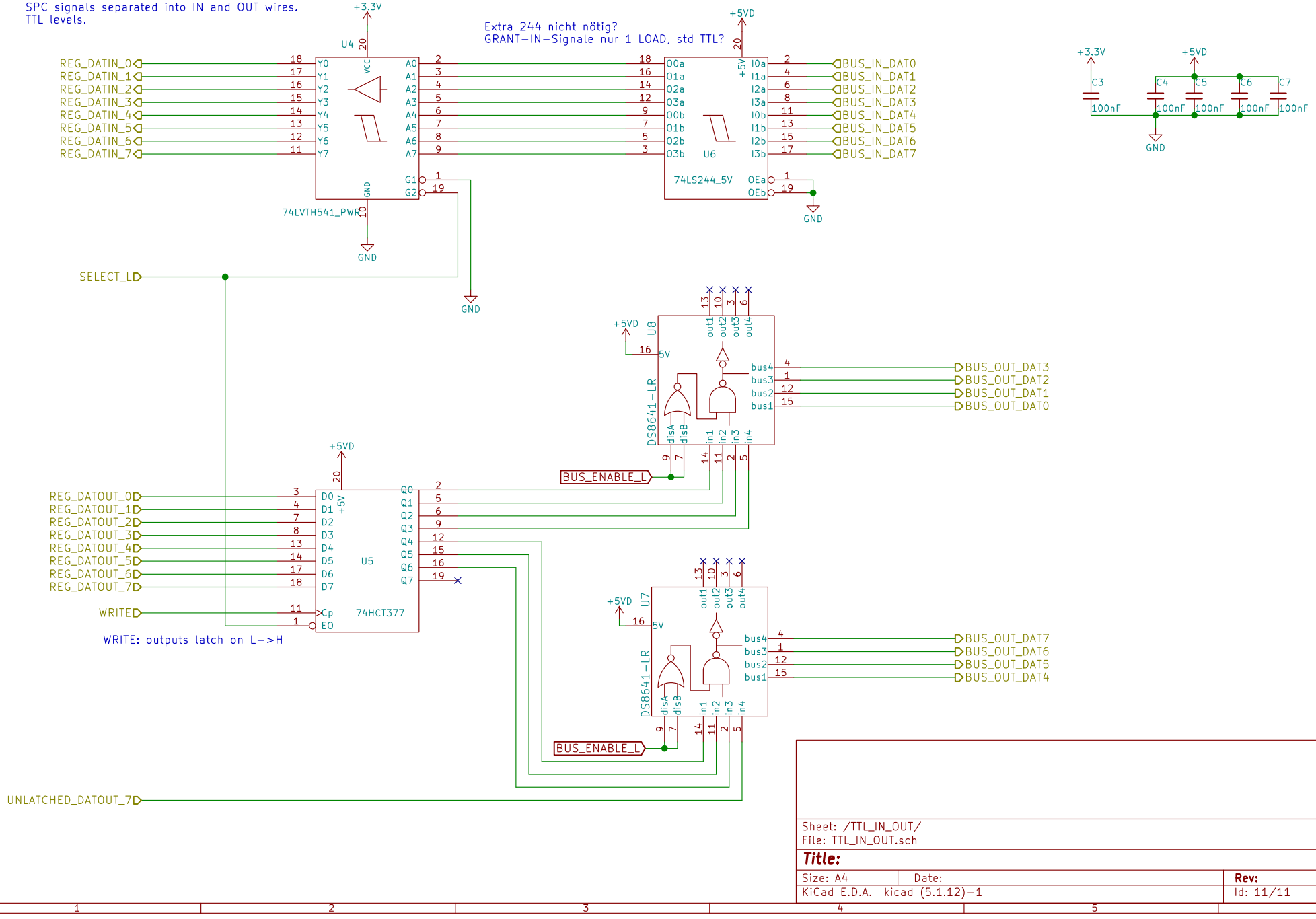

Sheet: /DS8641-DAT815/
File: DS8641.sch

**Title:**

| Size: A4 | Date: | **Rev:** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 10/11 |

SPC signals separated into IN and OUT wires.
TTL levels.

Extra 244 nicht nötig?
GRANT-IN-Signale nur 1 LOAD, std TTL?

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|---|---|---|
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| File: TTL_IN_OUT.sch | | |
| **Title:** | | |
| Size: A4 | Date: | **Rev:** |
| KiCad E.D.A. kicad (5.1.12)-1 | | Id: 11/11 |